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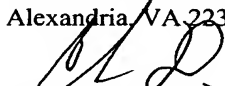
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Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Kae Hoon LEE**, a citizen of the Republic of Korea, residing at 6-258, Changjeon-dong, Mapo-gu, Seoul, Korea have invented new and useful **METHODS FOR FORMING A DEVICE ISOLATING BARRIER AND METHODS FOR FORMING A GATE ELECTRODE USING THE SAME**, of which the following is a specification.

METHODS FOR FORMING A DEVICE ISOLATING BARRIER AND METHODS FOR FORMING A GATE ELECTRODE USING THE SAME

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to semiconductor devices; and, more particularly, to methods for forming a device isolating barrier, and methods for forming a gate electrode using the device isolation barrier.

BACKGROUND

[0002] Conventional methods for forming a semiconductor device isolating barrier include a LOCOS (Local Oxidation of Silicon) method using a nitride layer and an STI (Shallow trench isolation) method which isolates devices by forming a trench on a surface of the semiconductor substrate.

[0003] Since the LOCOS method employs a simple process of thermal oxidization of a semiconductor substrate using a nitride layer as a mask, element stress of the oxide layer is small and the generated oxide layer has high quality. However, the device isolating region occupies a large area, thereby limiting the miniaturization of the semiconductor device. On the contrary, in the STI method, after a trench is formed on a surface of a semiconductor substrate, the trench is filled with an insulating film which is subsequently flattened. Accordingly, the STI method creates a small device isolating region, thereby having an advantage with respect to miniaturization of the semiconductor device.

[0004] Figs. 1A to 1F are cross-sectional views showing a conventional insulating method in which a trench is formed on a surface of a semiconductor substrate. As shown in Fig. 1A, after a pad oxide layer 2 having a thickness of about 150 Å is formed on a semiconductor substrate 1, a nitride layer 3 having a thickness of about 2000 Å is formed on the pad oxide layer 2. After a photoresist layer 4 is coated on the nitride layer 3, the photoresist layer 4 is exposed and developed to form a mask to create a trench, (i.e., a device isolating region), on a surface of the semiconductor substrate 1.

[0005] As shown in Fig. 1B, a trench T, (i.e., a device isolating region), is formed by etching the semiconductor substrate 1 to a depth of about 3000 Å to about 7000 Å and a width of about 300 Å to about 500 Å after etching the portions of the nitride layer 3 and the pad oxide layer 2 exposed through developing of the photoresist layer 4.

[0006] Referring to Fig. 1C, the trench T is filled by depositing a thick insulating layer 6, (i.e., an oxide layer), on a surface of the semiconductor substrate 1 by performing a CVD (chemical vapor deposition) process. Prior to performing the CVD process, a liner oxide layer 5 is formed inside the trench T such that the trench T makes good contact with the filling oxide layer 6 in the process of filling the trench with the insulating layer 6 and such that an edge of the trench is rounded.

[0007] Referring to Fig. 1D, after coating the insulating layer 6 with a photoresist layer 7, the photoresist layer 7 is exposed and developed by using a mask. As a result, the photoresist layer pattern 7 remains only on the insulating layer 6 above the trench T. An insulating layer pattern 6a is formed

by etching the insulating layer 6 using the photoresist layer pattern 7 as a mask.

[0008] As shown in Fig. 1E, after removing the photoresist layer pattern 7, a device isolating barrier 8, (i.e., flattened insulating layer pattern 6a), is formed by polishing and flattening the insulating layer pattern 6a to the height of the nitride layer 3 through a CMP (chemical mechanical polishing) process.

[0009] As shown in Fig. 1F, when the exposed nitride layer 3 is removed by wet etching using phosphoric acid, the semiconductor substrate 1 is divided into active regions at both sides of the device isolating barrier 8 and a device isolating region corresponding to the device isolating barrier 8.

[0010] In the conventional semiconductor device isolating method, the oxide layer and the nitride layer 3 are flattened, and then the exposed nitride layer 3 is removed by phosphoric acid. During the flattening of layers, an electric field is concentrated on a periphery A of the trench T, as shown in Fig. 1F, thereby causing the Kink effect, (i.e., leakage current generation at the trench T), which deteriorates the reliability and characteristics of the semiconductor device.

[0011] Although not shown in the drawings, after a gate electrode including a conducting layer is formed on the active region by using a general gate electrode forming method, drain/source regions are formed employing the gate electrode as a criterion by executing impurity ion implantation.

[0012] In this case, a problem occurs in that a device isolation resistance is changed since impurities are also doped inside the trench during

the impurity ion implantation to form the drain/source regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figs. 1A to 1F are cross-sectional views showing a conventional insulating method

[0014] Figs. 2A to 2K are cross-sectional views illustrating an example method for forming a gate electrode in accordance with the teachings of the present disclosure.

DETAILED DESCRIPTION

[0015] Figs. 2A to 2I are cross-sectional views illustrating an example method for forming a semiconductor device insulating barrier and an example method for forming a gate electrode.

[0016] Referring to Fig. 2A, a preferred example sequentially accumulates a pad oxide layer 102 and a first nitride layer 104 on top of a semiconductor substrate 100. Then, a photoresist layer is coated on the first nitride layer 104. Subsequently, a first photoresist layer pattern 106 is formed by removing the portion of the photoresist layer where a first trench will be formed through an exposure and developing process performed on the coated photoresist layer. The thickness of the first nitride layer 104 may range from about 500 to about 1000 Å.

[0017] As shown in Fig. 2B, after the pad oxide layer 102 and the first nitride layer 104 are etched by using the first photoresist layer pattern 106 as a mask, the first photoresist layer pattern 106 is removed. An oxide layer 108 is

then formed on the semiconductor substrate 100 to fill the holes etched in the pad oxide layer 102a and the first nitride layer 104a.

[0018] Next, as shown in Fig. 2C, oxide layer spacers 108a are formed at the sidewalls of the etched pad oxide layer 102a and the first nitride layer 104a by removing a part of the oxide layer 108 through an etch back process.

[0019] Then, as shown in Fig. 2D, the trench T is formed by etching the exposed semiconductor substrate 100 using the etched first nitride layer 104a and oxide layer spacer 108a as a mask.

[0020] As shown in Fig. 2E, after a liner oxide layer 110 is formed on the semiconductor substrate 100 and inside the first trench T, a trench oxide layer 112 is formed to fill the trench T.

[0021] Next, as shown in Fig. 2F, a device isolating barrier 112a is formed by removing the trench oxide layer 112 and the liner oxide layer 110 through a flattening process. As a result of the flattening process, the etched first nitride layer 104a is exposed and the trench oxide layer 112 is left only inside the first trench T. A CMP process may be applied as the flattening process.

[0022] Referring to Fig. 2G, a second nitride layer 114 is formed on the structure of Fig. 2F. A second photoresist layer pattern 116 to define a gate region is then formed on the second nitride layer 114. The thickness of the second nitride layer 114 may range from about 1000 to about 1500 Å.

[0023] As shown in Fig. 2H, after a second trench T' is formed by etching the second nitride layer 114 and the etched first nitride layer 104a using the second photoresist layer pattern 116 as a mask, the second

photoresist layer pattern 116 is removed. When the second trench T' is formed, an etching gas is used which has a selectivity of a multi-layer structured nitride layer (composed of the second nitride layer 114 and the etched first nitride layer 104a) with respect to the oxide layer that is greater than 7 : 1, (e.g., a gas mixture of CO, CHF₃ and C₄F₈).

[0024] As shown in Figs. 2I and 2J, a conducting layer 118 is formed to fill the second trench T'. Subsequently, the conducting layer 118 is removed through a flattening process to again expose the second nitride layer 114. A doped polysilicon or an undoped polysilicon may be used as the conducting layer 118. The conducting layer 118 may be deposited to fill the second trench T' through a LPCVD (low-pressure chemical vapor deposition) process at about 550 to about 650°C. The thickness of the deposited conducting layer 118 may range from about 2000 to 5000 Å.

[0025] The flattening process is executed using a CMP method. The thickness of the nitride layer left after the flattening process ranges from about 10 to about 90 % of the thickness of the nitride layer before the flattening process. During the flattening process, the thickness of the conducting layer 118 can be modulated by using an EPD (endpoint detector) system of a chemical mechanical polishing device.

[0026] As shown in Fig. 2K, a gate electrode 118a is formed by removing the second nitride layer 114 and the etched first nitride layer 104a through an etch back process. In the illustrated example, phosphoric acid is used to remove the second nitride layer 114 and the etched first nitride layer 104a.

[0027] From the foregoing, persons of ordinary skill in the art will appreciate that example methods for forming a semiconductor device isolating barrier capable of suppressing current leakage at a periphery of a trench generated in forming the device isolating barrier in a semiconductor substrate have been disclosed. The methods illustrated herein improve the reliability and the characteristics of the manufactured semiconductor device.

[0028] Further, persons of ordinary skill in the art will appreciate that example methods for forming a gate electrode of a semiconductor device capable of increasing yield and reducing manufacturing cost by simplifying the gate electrode forming process have been provided. In the illustrated examples, a gate electrode is formed by using a pad oxide layer and a nitride layer; both of which are formed during the trench forming process.

[0029] A preferred example method illustrated herein includes: sequentially forming a pad oxide layer and a first nitride layer on top of a semiconductor substrate; forming a trench region by etching the pad oxide layer and the first nitride layer; forming spacers at sidewalls of the etched pad oxide layer and the etched first nitride layer; forming a first trench by etching the semiconductor substrate using the spacers and the etched first nitride layer as a mask; and, after forming a liner oxide layer and an oxide layer filling the trench on the semiconductor substrate, forming the device isolating barrier by flattening the liner oxide layer and the trench oxide layer to expose the etched first nitride layer.

[0030] An another example method for forming a gate electrode of a semiconductor device comprises: sequentially forming a pad oxide layer and a

first nitride layer on top of a semiconductor substrate; forming a trench region by etching the pad oxide layer and the first nitride layer; forming spacers at sidewalls of the etched pad oxide layer and the etched first nitride layer; forming a first trench by etching the semiconductor substrate using the spacers and the etched first nitride layer as a mask; after forming a liner oxide layer and an oxide layer filling the first trench, forming the device isolating barrier by flattening the liner oxide layer and the trench oxide layer to expose the etched first nitride layer; after forming a second nitride layer on top of the etched first nitride layer, forming a second trench by etching the second nitride layer and the etched first nitride layer; after a conducting layer is formed to fill the second trench, flattening the conducting layer by removing the conducting layer to expose the second nitride layer; and forming the gate electrode by removing the second nitride layer and the etched first nitride layer.

[0031] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.